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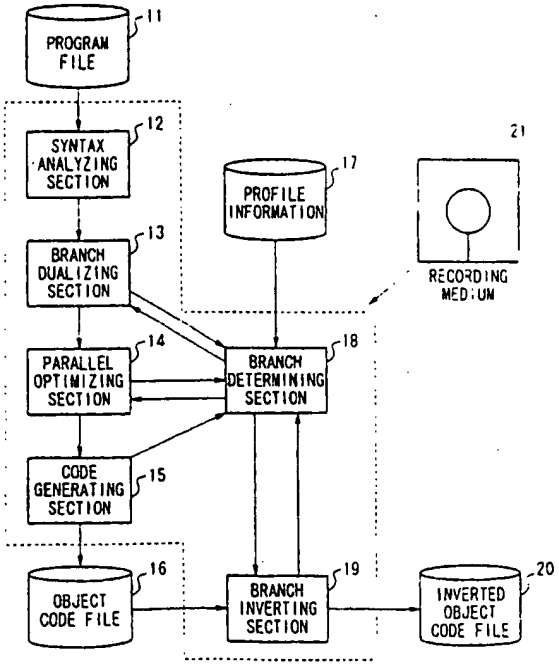
(54) Method and apparatus for compiling program for parallel processing, and computer readable recording medium recorded with parallelizing compilation program

(57) A parallelizing compilation apparatus for generating object codes that can execute processing, which begin at the branch target where control transfers with higher probability, in advance of the execution of a conditional branch instruction in parallel with the processing prior to the conditional branch instruction without the rearrangement of basic blocks is provided. A branch dualizing section (13) determines, based on profile information (17), the truth probability of the evaluation value of the conditional expression in a conditional branch instruction included in intermediate codes. When the probability of "false" is higher, the branch dualizing section dualizes the conditional branch instruction into a conditional branch instruction whose conditional expression is the inversion of that in the dualized conditional branch instruction and whose branch target is the next instruction of the dualized conditional branch instruction. Conversely, when the probability of "true" is higher, the branch dualizing section inserts an unconditional branch instruction just after the dualized conditional branch instruction and sets the branch target thereof to the next instruction of this unconditional branch instruction. A branch inverting section (19) generates object codes in which the target address of conditional branch instructions and unconditional branch instructions are exchanged, when the determination relating to the truth probability using profile information is inverted with respect to that at the time of the generation of an object code file (16).

FIG. 1



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EUROPEAN SEARCH REPORT

Application Number
EP 00 12 2314

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
A,D	SAKAI J: "Automatic parallelizing method for control-parallel multi-threaded architecture" TRANS. INF. PROCESS. SOC. JPN., vol. 40, no. 5, May 1999 (1999-05), pages 2045-2053, XP008029532 * abstract; figure 2 *	1-13	G06F9/45 G06F9/32 G06F9/38
A	US 5 659 752 A (HEISCH RANDALL RAY ET AL) 19 August 1997 (1997-08-19). * abstract * * column 1, line 23-25 * * column 5, line 5-22 * * column 5, line 43 - column 6, line 24 *	1-13	

TECHNICAL FIELDS SEARCHED (Int.Cl.7)

G06F

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	19 April 2004	Uhlmann, N

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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19-04-2004

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5659752 A	19-08-1997	NONE	

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For more details about this annex : see Official Journal of the European Patent Office, No. 12/82